Speech subject： Metal/Dielectric Hybrid Bonding for Heterogenous Integration Applications

Speech leader: V. Dragoi—Chief Scientist, EV Group

Speech Description/Objective:

Hybrid wafer-to-wafer bonding gained over the past decade a significant interest as it can provide major advantages in fabrication of wafer-level interconnects. As an alternative process, die-to-wafer process flows were developed. The process is extremely challenging in terms of surface preparation, as substrates must accommodate two types of bonding processes simultaneously (dielectric-dielectric and Cu-Cu bonding at bonding pad level). The fabrication of the bonding surfaces has to produce a specific topography (metal recess with respect to dielectric surface within single digit nanometers, dielectric surface with very low microroughnes – less than 0,5 nm, etc,) with very high uniformity across wafers up to 300 mm diameter. The bonding process has to ensure a high alignment accuracy (sub-micrometer) across the entire wafer and low temperature processing, within the CMOS thermal budget (<400°C). After the bonding process one of the two bonding partners has to be thinned down: in case the substrates preparation was not performed according to specifications or the bonding process was not properly performed, the structures on the wafer will be distorted, making further processing more difficult, time consuming and adding costs. Thus, substrates quality and accurate bonding process control are of a very high importance.

A. Wafer-to-Wafer Bonding

In order to perform dielectric/metal hybrid wafer bonding the wafers require a special preparation. Such wafers will exhibit a large area of dielectric material (e.g. various CVD-deposited SiO2, SiC or SiCN) with small metal “islands”, the Cu pads (see Fig. 1). The final goal of the process is to have a strong bond between the two dielectric surfaces and a Cu-Cu bond ensuring the metal interconnects at wafer level.

The bonding process flow is similar to low temperature fusion bonding process [1]: first the wafers are activated in plasma, then cleaned with water for airborne particles removal, optically aligned and placed in contact at room temperature inside the optical alignment equipment, to minimize the risk of inducing misalignment due to additional handling steps.

The process results are assessed first by optical alignment accuracy. An overlay model is proposed to allow for large area alignment accuracy assessment to allow for high accuracy (currently <150 nm accuracy is reachable in production).

B. Die-to-Wafer Bonding

The high production yield required by some applications would be hard to reach in a wafer-to-wafer process. For such cases, one wafer is bonded to dies singulated from a second

wafer and selected based on a “known good die” principle: this way, the two wafers’ individual yields will not further impact on the bonded pair’s yield.

While the bonding process is identical to the above illustrated wafer-to-wafer flow, two alternative process flows are available with respect to dies handling (Fig.2.): a standard pick-and-place method and collective die-to-wafer method [].

Fig.3. presents a photography of a wafer showing dies of different dimensions bonded, and a cross section of a hybrid die-to-wafer bond.

The process flows will be explained in detail and illustrated with experimental results. The main challenges will be described and future applications based on hybrid bonding will be described.

Keywords: Heterogenous Integration; Chiplets; Hybrid Bonding

Fig. 1. Hybrid bonding schematic process flow: CMOS wafers planarization, surface activation, optical alignment, spontaneous dielectric-dielectric fusion bonding by contact, and thermal annealing resulting in Cu-Cu metal thermo-compression bonding (no contact pressure applied, the high pressure required is provided by Cu thermal expansion during annealing.

Fig. 2. Die-to-wafer hybrid bonding process flows.

Fig.3. Die-to-wafer bonding results: TEM cross section of a hybrid bond
showing the high quality of the Cu-Cu pads bond.

Conclusion

1. Hybrid bonding represents already a mature technology which can be used for a large variety of applications.
2. Die-to-wafer bonding technology is a versatile technique allowing for chiplet integration in heterogenous integration applications.